SECTION 6

TROUBLESHOOTING

6.0 SELF-DIAGNOSTIC FEATURES

The Model 115 Fetal Monitor incorporates a number of internal self-diagnostic features designed to assist the biomedical engineer in verifying the unit's performance at major component and printed circuit board levels. These features, and knowledge of the monitor's operating characteristics, provide a means to troubleshoot at circuit board level using standard Model 115 accessories, a digital voltmeter, and a clip lead.

The following Model 115 Fetal Monitor features can be used to assist troubleshooting and/or repairing of the unit.

- Front-panel Test button
- $2^1/_2$-digit UA display
- Rear-panel FECG simulator
- Main CPU Board self-test software
- Recorder CPU Board self-test software
- Correlator CPU Board self-test software
- Main CPU Board event trigger indicator

6.1 FRONT-PANEL TEST BUTTON

Depressing the monitor's front-panel Test button initiates a sequence of self-test routines which are intended to verify the functional capability of the following subsystems:

1. Main CPU Board (5802 or 6802) system clock (6.144 MHz), time base (1.1 kHz derived from 2.3 MHz) and 8085 microprocessor.
2. Main CPU Board front-panel display and switch I/O ports.
3. Front-panel display and indicator circuits (5812).
4. Main CPU Board (5802 or 6802) and Recorder CPU Board digital communication I/O ports and handshaking circuitry.
5. Recorder CPU Board system clock (6.144 MHz), time base (9 kHz derived from 2.3 MHz) and 8085 microprocessor.
6. Recorder CPU Board stepper-motor driver and printhead output circuitry.
7. Thermal printhead and paper-out detector circuitry.
8. Main CPU Board (5802 or 6802) and uterine activity analog-to-digital conversion and input circuitry (5800 Board).

Failure of the Model 115 Fetal Monitor to activate the appropriate front-panel indicators or, to print the specified chart recorder test pattern, generally indicates a malfunction in one of the above mentioned circuits. Also, failure of the recorder to print may be due to an absence of chart paper, recorder door open, or a malfunction of the recorder's PAPER-OUT sensor circuitry.

6.2 REAR-PANEL FECG SIMULATOR

The Model 115 Fetal Monitor includes a rear-panel mounted leg-plate tester jack which is connected to an internal FECG Simulator. This simulator continuously outputs a 500 μV, 120 BPM simulated fetal R-wave and can be used to verify leg-plate wiring integrity, as well as, its preamplifier, ECG processing and cardiotachometer circuitry.

Once the leg plate has been attached to the test jack, a properly functioning monitor will begin to count heart rate at 120 ± 1 BPM after a short stabilization period. Failure of the Model 115 Fetal Monitor to count heart rate under this condition indicates a malfunction in one of the following areas:

- Broken leg-plate cable or connector wires.
- Malfunctioning front-panel ECG connector harness.
- Defective FECG preamplifier and/or QRS detector circuitry (5806 or 5807 Board).
- Defective Main CPU cardiotachometer circuitry (6802 Board).
- No 36 kHz (5800 Board).

When the monitor fails to count heart rate with the leg plate properly connected, the leg-plate cable wiring continuity should be checked first. This is the first step in troubleshooting a direct ECG mode malfunction since the most likely cause would be a broken leg-plate cable wire. If the leg plate is found to be functional, observation of the Event Trigger LED mounted on the Main CPU Board (6802) will indicate the unit's analog ECG circuitry is functional by flashing at 120 BPM. If the Event Trigger LED does not flash, a malfunction is indicated in the FECG preamplifier, QRS detector circuitry, front-panel harness, or on the boards (5806, 5807) housing the FECG enable circuitry. Consistent flashing of this LED in the absence of counting suggests a defective Main CPU Board; a condition which can be further evaluated using the Main CPU Board self-test software.

6.3 MAIN CPU BOARD SELF-TEST SOFTWARE (5802 or 6802)

Description

The Model 115 Fetal Monitor's Main CPU Board contains self-test capabilities which allow board level confidence testing. The 8085 microprocessor controls the test and sequentially checks each major CPU board component, as well as, the CPU-Recorder interface. Detection of a major CPU component failure is indicated by a specific code which appears on the front-panel heart rate display.

NOTE: Front-panel LED's may blink during self-test.

Procedure

The CPU Board's self-test is activated by connecting a jumper between the appropriate test point (see TABLE 6-1) and TP1 (GND). These test points must remain grounded throughout the test. The on-board test LED illuminates to indicate activation of the self-test.

NOTE: Prior to activation of the CPU self-test on dual-cardiotach monitors, a legplate as well as either an ultrasound or phono transducer must be inserted.

CPU BOARD	TEST POINT
5802C	JA
5802D	TP2
6802J	TP2
all other boards	U7 (pin 16)

CPU TEST POINTS
TABLE 6-1

The tests are divided into two categories: internal CPU board component test and CPU-Recorder interface test. As each CPU component test is executed, its assigned sequence number appears in the front-panel display window as described previously. Once a component failure is sensed and displayed, the remaining self-test routines are inhibited. Successful completion of the component test is indicated by 1-Hz flashing of the test LED. However, this will only occur after completion of the CPU-Recorder interface test.

Component Test Sequence

The component test sequence numbers, test descriptions, and approximate execution times are outlined in TABLE 6-2. Read the following note carefully prior to initiating the self-test.

NOTE: During Test 6, the CPU loads a predetermined value into the 8155 timer and tests for a decremented count after a specified interval. Decrementing of the timer is controlled by the pressure V/F converter output. If a tocotransducer or strain gauge is not plugged into the front-panel UA receptacle, the pressure V/F converter output is unpredictable and may cause an erroneous failure indication during Test 6. Therefore, it is a requirement that either a toco or strain gauge be plugged into the UA connector during the self-test.

The main CPU automatically undertakes the CPU-Recorder interface test upon successful completion of the CPU component tests. Upon initialization of the interface test, a prescribed heart rate and uterine activity pattern is transmitted to the Recorder CPU Board. Heart rate values are simultaneously displayed on the monitor's front-panel display screen.

Sequence No.	Description	Execution Time
1	**8085 Processor Test** CPU checks itself by testing all of its internal registers, arithmetic and logical operations and its ability to alter program flow with "JUMP" and "CALL" instructions. **NOTE:** A faulty systems clock or seriously malfunctioning RAM or ROM may cause a failure during this test.	1 second
2	**Read Only Memory Test** A cyclic redundancy check is performed on the entire ROM contents as a check that all bytes are still as originally programmed.	9 seconds
3	**Main Random Access Memory Test** Special bit patterns are written to and read from the system RAM to verify bit-wise integrity. **NOTE:** This test does not assure integrity of the CPU's addressing system.	1 second
4	**Clock Random Access Memory Test** Same as Sequence Test #3 except test is performed on Real Time Clock RAM.	1 second
5	**Real Time Clock Test** Sets real time clock to a specified time and date then tests that values were incremented one second later. Tests internal real time clock alarms	2 seconds 2 seconds
6	**8155 Timer Test** Loads the 8155 timer register with a predetermined value and after a fixed delay, checks for a decremented count. **NOTE:** This test requires that a toco or strain gauge transducer be connected to the monitor's front panel. **NOTE:** Failure of this test may be caused by malfunction of the Model 115's 2.3 MHz oscillator or its frequency division circuitry.	1 second

SELF-TEST SEQUENCES – MAIN CPU BOARD
TABLE 6-2

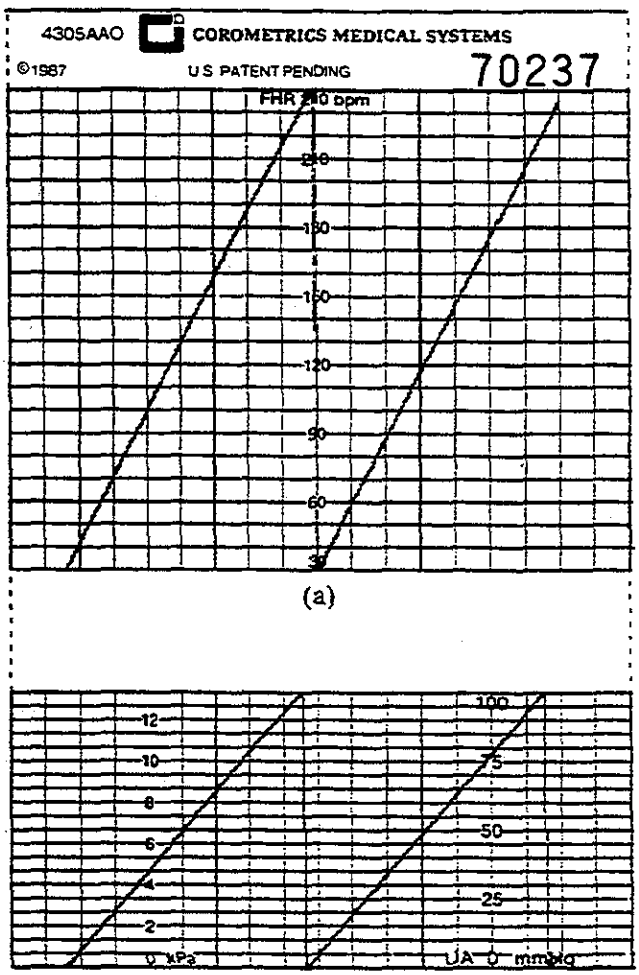
If the Recorder CPU Board is functioning properly (as determined by Recorder CPU self-test), successful printing of the HR/UA pattern will occur as depicted in FIGURE 6-1 (single-cardiotach) and FIGURE 6-2 (dual-cardiotach). Such a printout indicates a properly functioning CPU-Recorder interface.

NOTE: On dual-cardiotach monitors, the second HR ramp is 3 dots wide indicating dual-cardiotach operation.

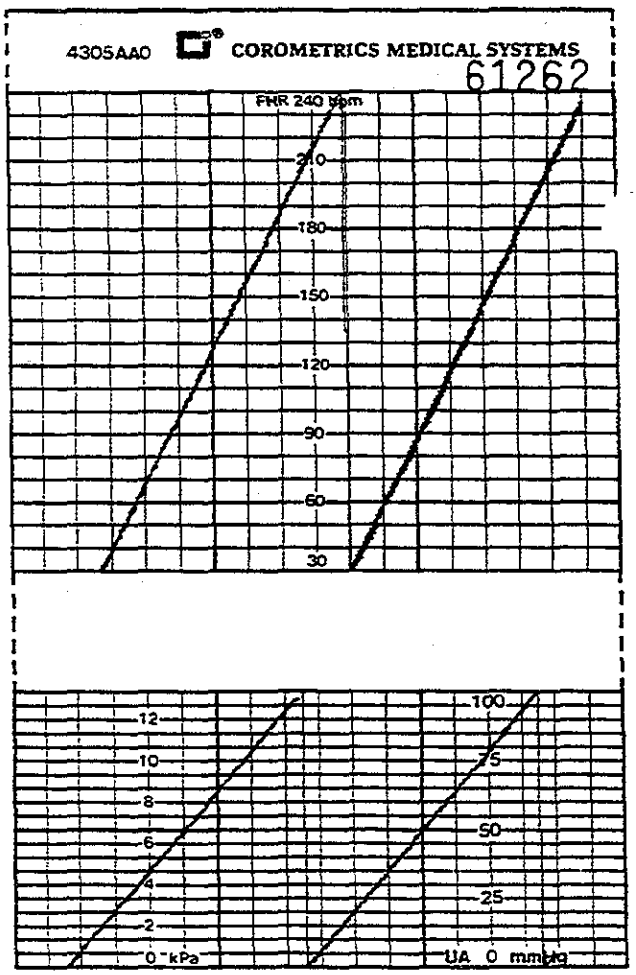
6.4 RECORDER CPU BOARD SELF-TEST SOFTWARE (5808, 6709, 6808, 6665, 6666)

Description

The Recorder CPU Board self-test feature allows for confidence testing of the Recorder CPU Board, recorder's thermal printhead, and stepper-motor circuitry. These tests are controlled by the CPU Board's 8085 microprocessor which sequentially checks each major CPU component and the unit's printhead output circuitry. When a major CPU component failure is detected it is so indicated by a printed message on the strip-chart record.



HR/UA PATTERN - 5802 BOARD
FIGURE 6-1



HR/UA PATTERN - 6802 BOARD
FIGURE 6-2

6.4.1 RECORDER CPU BOARD W/O RS-232C OPTION (5808, 6709, and 6665 Boards)

Procedure

Once the monitor has completed its power-up sequence, the board's self-test software can be activated by using a jumper to connect TP9 to TP10. The recorder will automatically be activated and will turn off upon completion of the test. The on-board test LED will be illuminated continuously while the self-test is in progress, and will flash at 1 Hz upon successful completion of all tests.

Note: Jumper must remain connected throughout test.

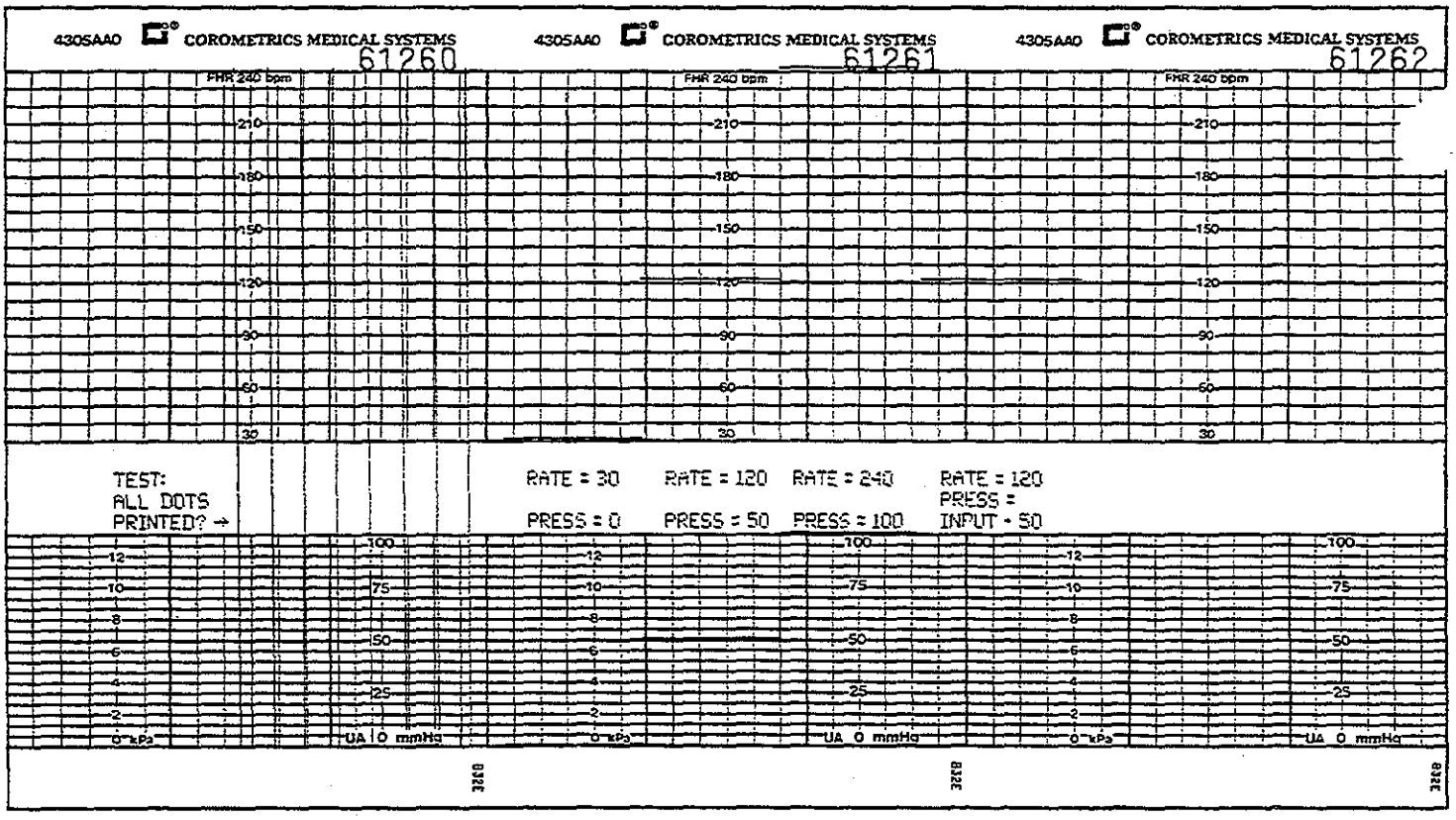
Recorder board testing is divided into two categories: recorder printing test and internal CPU component test. Since the strip-chart recorder is used to identify failed components, the recorder CPU's output circuitry, printhead, and stepper-motor drive circuits are self-tested first.

Self-Test Sequences

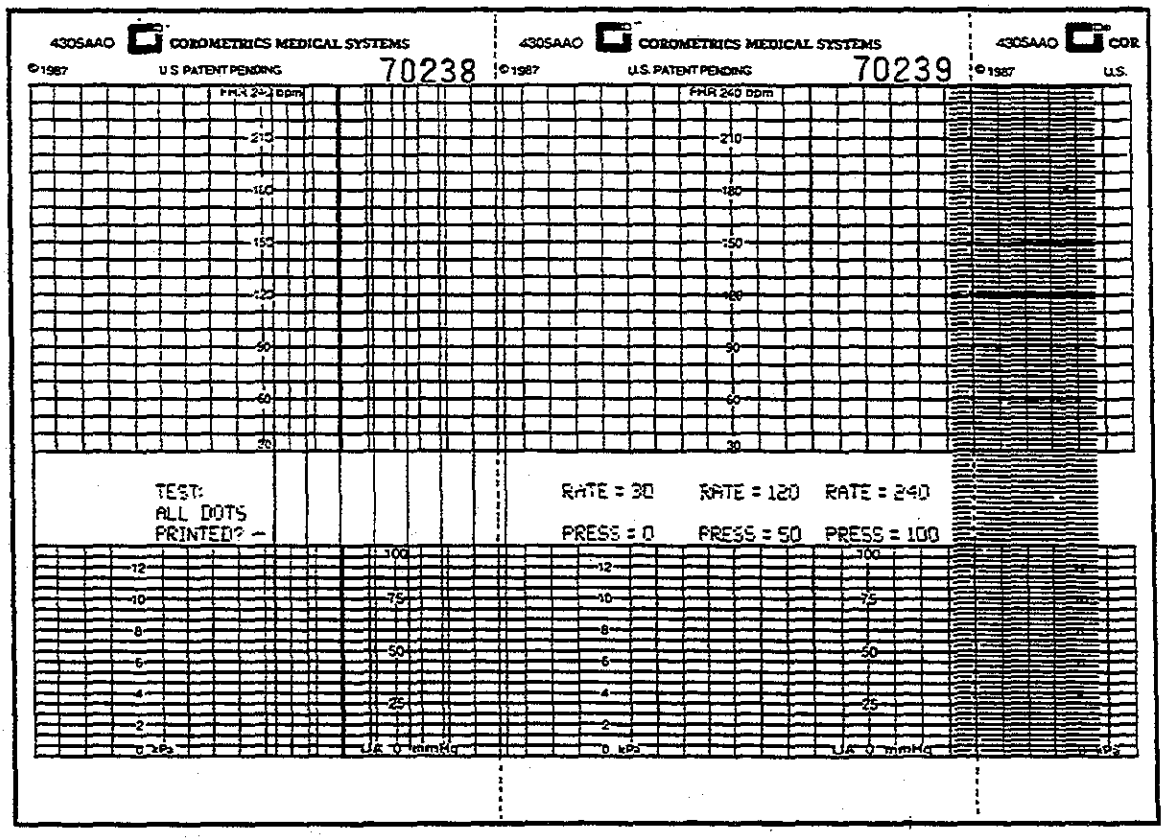
The recorder CPU's sequence of self-tests and expected results, respectively, are outlined in TABLE 6-3.

Test No.	Description
1	**Recorder Printing Test** Comprehensive recorder CPU test which causes a predetermined pattern to be printed on the strip-chart record. (See FIGURE 6-3.) Successful completion of this test requires minimal 8085, RAM and ROM functionality as well as proper function of the recorder printhead, stepper motor, and CPU output circuitry. (Proper function of the Main CPU recorder interface is not required for successful completion of this test.) Complete failure of the recorder to print and advance paper generally indicates a paper-out sensor circuit failure, an 8085 CPU or systems clock failure (6 MHz or 2.3 MHz) or a ROM failure. Printing of a garbled strip-chart pattern suggests a RAM, output circuit, or printhead failure.
2	**8085 Processor Test** CPU checks itself by testing all of its internal registers, arithmetic and logical operations, and its ability to alter program flow with "JUMP" and "CALL" instructions. If an error is detected, the processor will attempt to print the message "8085 ERROR" on the chart. The test lamp will never flash if such an error is detected.
3	**Random Access Memory Test** Special bit patterns are written to and read from the board's 8155 RAM to verify bitwise integrity. Detection of a RAM error will cause the "RAM ERROR" message to be printed on the strip-chart record. Flashing of the test lamp will be permanently inhibited if such an error is detected.
4	**Read Only Memory Test** A cyclic redundancy check is performed on the entire ROM contents to ensure that all bytes remain as originally programmed. Failure of this test will cause "ROM ERROR" to be printed and will inhibit flashing of the test LED.
5	**Printhead Loader Hardware Test** Optional test activated by depression of the front-panel "Paper Advance" button while the jumper is still connected. Causes the recorder CPU to activate every fourth element of the thermal printhead. Provides a stable recorder output circuit waveform for troubleshooting output hardware faults. (See FIGURE 6-4.)

SELF-TEST SEQUENCES — RECORDER CPU W/O RS-232C
TABLE 6-3



COMPREHENSIVE RECORDER CPU TEST PATTERN
FIGURE 6-3

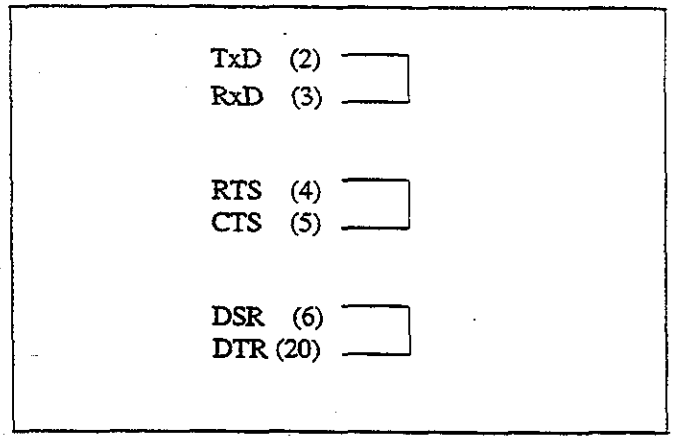


OPTIONAL RECORDER CPU TEST PATTERN
FIGURE 6-4

If the recorder CPU Board provides the RS-232C option, an extensive internal test may be performed.The first portion of the test is identical to the Recorder CPU test without the RS-232C option. The second portion is the RS-232C Interface test.

Procedure

1. To enable the RS-232C Interface portion of the test, a jumper must be placed between TP15 and TP10. To ensure correct operation of the test, the Baud Rate selector switch should be placed in the 9600 or 4800 position.
2. In order for the test to function properly, a special loopback connector must be inserted into the rear-panel RS-232C connector. This connector should be installed prior to activation of the test. The layout of this connector is shown in FIGURE 6-5.



LOOPBACK TEST CONNECTOR
FIGURE 6-5

3. Following completion of the power-up sequence, both portions of the self-test are activated by connecting a jumper between TP9 and TP10. An on-board LED will illuminate indicating the self-test is in progress.

Note: All of the above must be performed for the recorder to activate.

Self-Test Sequences

The Recorder CPU performs the same sequence of tests listed in TABLE 6-2 as well as the RS-232C Interface test sequences outlined in TABLE 6-4.

Test No.	Description
1	**DSR Test** The current state of DSR is checked to make sure this line is asserted (looped back from DTR).
2	**Transmitter Test** The state of the transmitter is checked to make sure it is ready to transmit a data byte. (This indirectly checks that CTS is asserted.)
3	**Byte Transmission Test** A byte is transmitted.
4	**Byte Receiver Test** After a delay, the receiver is checked to make sure the byte has been received.
5	**Byte Comparison Test** The received byte is compared to the transmitted byte.
6	**Second Data-Byte Test** Tests 2-5 are repeated for a second data byte.

RS-232C INTERFACE TEST
TABLE 6-4

Upon successful completion of the RS-232C self-test, the self-test LED will flash. RS-232C failure is indicated by a message printed in the lower right corner on the strip-chart recorder; the message will read "RS-232 ERROR". If an RS-232C failure does occur, the optional Printhead Loader Hardware Test cannot be performed.

6.5 CORRELATOR CPU BOARD SELF-TEST SOFTWARE (5801 or 7180)

The Correlator CPU Board self-tests include a board level confidence testing carried out under the control of the board's CPU microprocessor which sequentially checks each major CPU component and the Correlator-Main CPU interface. When possible, failure of a major CPU component is indicated by a voltage level present at the output of the optional 5803 Test Board which attaches to the Correlator Board (5801 or 7180).

6.5.1 5801 BOARD

Procedure

The 5801 Board's self-test software is divided into two separate and distinct sections, each of which operates independently of the other and is activated by a different mechanism.

1. The first group of 5801 Board self-test routines is activated by connecting TP3 to TP1 (+5 V) after the Model 115 has completed its power up sequence. These routines perform an internal component test and are activated in the sequence outlined in TABLE 6-4. Making this connection causes the on-board test LED to illuminate indicating that a CPU test is in progress. The LED will begin flashing after approximately 30 seconds if no failures were detected during the self-test.

Test No.	Description
1	**8085A-2 Processor Test** The CPU checks itself by testing all of its internal registers, arithmetic and logical operations, and its ability to alter program flow with "JUMP" and "CALL" instructions. **NOTE:** A faulty systems clock or a seriously malfunctioning RAM or ROM may cause a failure during this test.
2	**9114A Random Access Memory Test** Special bit patterns are written to and read from each of the two 9114 RAM chips to verify bit-wise integrity. **NOTE:** This test does not assure integrity of the CPU's RAM addressing system.
3	**Read Only Memory Test** A cyclic redundancy check is performed on the entire ROM contents as a check that all bytes are as originally programmed.
4	**8156 Random Access Memory Test** Same as Test 2 except performed on 8156 RAM.
5	**Multiplier/Accumulator Test** Multiplier/Accumulator chip is tested by multiplying all combinations of numbers between 0 and 255 with verification of the results. Three MSB's of accumulator portion are also tested for functionality.

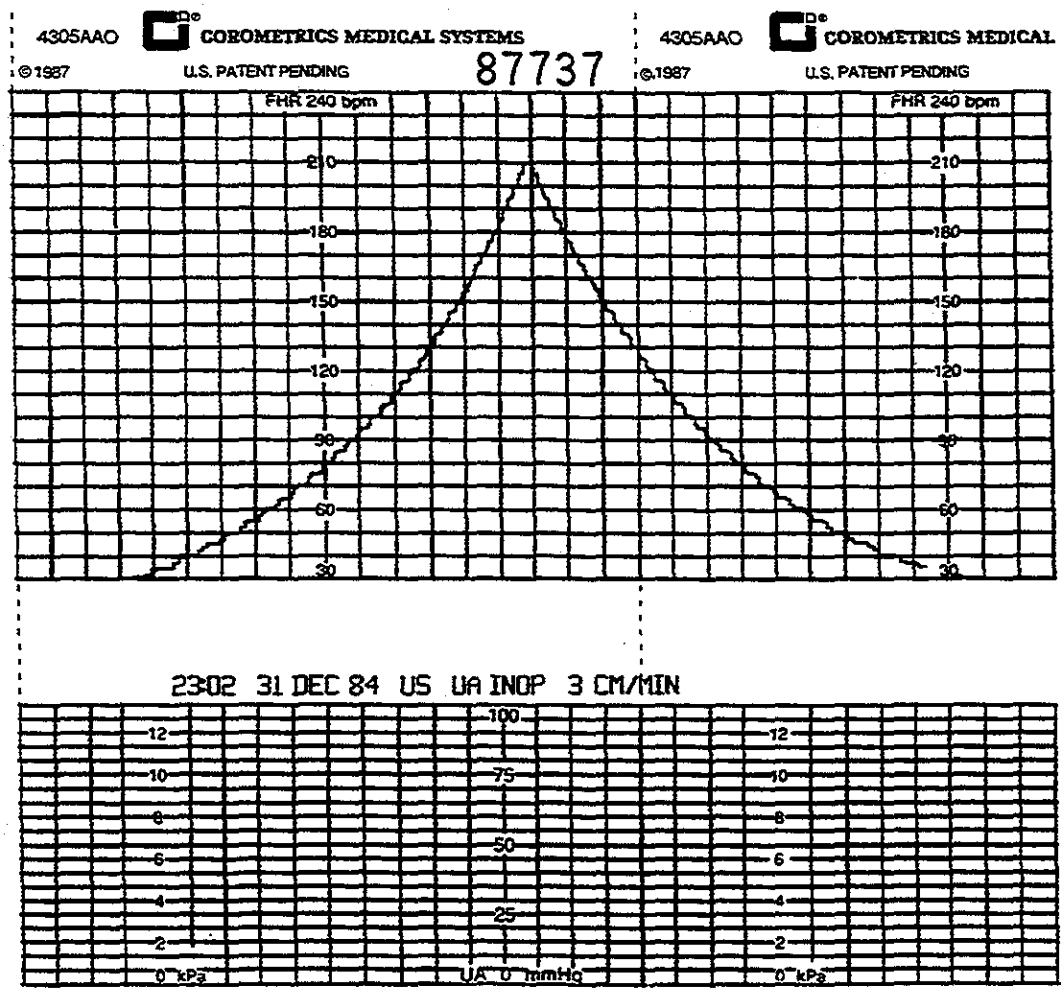
SELF TEST SEQUENCES — 5801
CORRELATOR CPU BOARD
TABLE 6-4

Failure of any of the above tests will inhibit flashing of the "TEST" LED following completion of the test sequenced. Thus, if after 30-45 seconds the LED does not flash, a CPU component failure has been detected. In this case, the nature of the component failure can be determined using an oscilloscope attached to the "Output" test point of the optional 5803 DAC Board which attached to the 5801 Board. If a test has failed, the processor will output a square wave whose low value, as a percentage of its high value, reflects the failed component according to TABLE 6-5.

Low Output Voltage / High Output Voltage	Failed Component
0%	8085A-2 Processor
20%	9114 RAM
40%	ROM
60%	8156 RAM
80%	Multiplier

FAILED COMPONENTS — 5801 CORRELATOR CPU
TABLE 6-5

2. The second group of 5801 Board self-test routines are activated by connecting TP4 to TP1 (+5 V) after the Model 115 has completed its power-up sequence. The routines activated in this way cause the Correlator CPU to generate a series of event triggers which are transmitted to the Main CPU Board for heart rate counting. This self-test routine permits checking of the event trigger output circuitry and the Main CPU Board for heart rate counting. This self-test routine permits checking of event trigger output circuitry and the Main CPU Board event input circuits. If an ultrasound transducer is connected to the Model 115's front-panel connector and the unit's recorder is activated, this test will produce the heart rate pattern illustrated in FIGURE 6-6.



HEART RATE PATTERN – ULTRASOUND TRANSDUCER
FIGURE 6-6

6.5.2 7180 BOARD

The Correlator CPU Board self-tests include a board level confidence test of the 7180 printed circuit board. The self-tests are controlled by the board's CPU microprocessor which sequentially checks each major CPU component and the Correlator-CPU interface. When a voltage level is presented at the output of a 5803 Test Board (which attaches to the 7180 Correlator), failure of a major CPU component is indicated.

Procedure

The 7180 Board's self-test routines are divided into two separate and distinct sections. Each section operates independently of the other and is activated by a different mechanism.

1. The first section performs internal component tests as outlined in TABLE 6-7. This first set of self-test routines is activated by connecting TP1 to TP3 (+0 V) after the Model 115 Fetal Monitor has completed its power-up sequence. Making this connection causes the on-board LED to illuminate, indicating the CPU test is in progress. Upon successful completion of the self-test, the Correlator Test LED will flash 15 times before resetting and returning to normal operation.

Test No.	Description
1	**6116 Random Access Memory Test** Special bit patterns are written to and read from each of the two 9114 RAM chips to verify bit-wise integrity. **NOTE:** This test does not assure integrity of the CPU's RAM addressing system.
2	**Read Only Memory Test** A cyclic redundancy check is performed on the entire ROM contents as a check that all bytes are as originally programmed.

SELF-TEST SEQUENCES — 7180 CORRELATOR CPU BOARD
TABLE 6-7

Failure of any test outlined in TABLE 6-7 will inhibit flashing of the test LED following completion of that test. Thus, if after 30-45 seconds the LED does not flash, a CPU component failure has been detected. In this event, attach an oscilloscope to the output test point of the 5803 DAC board to determine the nature of component failure. The processor outputs a square wave whose low value as a percentage of its high value reflects the "failed component" as shown in TABLE 6-8.

Low Output Voltage / High Output Voltage	Failed Component
20%	6116 RAM
40%	ROM

FAILED COMPONENTS — 7180 CORRELATOR CPU
TABLE 6-8

2. The second section, or group, of routines in the 7180 Board's self-test, is activated by connecting TP4 to TP3 (+5 V) after the monitor has completed its power-up sequence. Routines activated in this way cause the Correlator CPU to generate a series of event triggers which are transmitted to the main CPU Board for heart rate counting. This self-test routine permits checking of the event trigger output and the main CPU input circuitries. If an ultrasound transducer is connected to the Model 115 Fetal Monitor's front-panel connector, with unit's recorder activated, this test will produce a heart rate pattern as depicted in FIGURE 6-6.

During this test, the main CPU Board event trigger LED will flash with each simulated event pulse output by the Correlator Board. Simultaneously, the monitor's heart rate display will indicate the appropriate FHR value. Ultrasound audio, however, will not be heard from the rear-panel speaker.

The Correlator Test LED will illuminate at the start of the test. Upon successful completion of the self-test, the LED will flash 15 times before resetting and returning to normal operation. A CPU component failure will inhibit flashing of the self-test LED.

6.6 MAIN CPU BOARD EVENT TRIGGER INDICATOR

The Model 115 Fetal Monitor's Main CPU Board includes three LED indicators for monitor troubleshooting, a self-test LED, and two event trigger indicator LEDs which flash with each trigger received from the ECG Processor (5806 and 5807) or the Correlator CPU (7180) Board, respectively.

The CPU Board's event trigger LEDs allow service personnel to quickly determine if a monitor malfunction is in the monitor's signal processing subsection or the heart rate counting/strip chart recorder section.

If the CPU Board does not receive any event triggers during the monitoring mode or with simulated input signals, the event LEDs will not flash. This indicates a malfunction in the unit's signal processing circuitry or mode enable circuitry.

However, if triggers are recieved at the CPU Board (the event lamp will flash at the appropriate rate), the malfunction will be isolated within the Main CPU or Recorder CPU circuitry. (Refer to Section 5.7 for Recorder Board identification.)